IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
HIGETA et al.	)	
	)	
Application Number: To be Assigned	)	
	)	**Art Unit 2824**
Filed: Concurrently herewith	)	
	)	
For: SEMICONDUCTOR MEMORY DEVICE	)	
	)	
Attorney Docket No. HITA.0437	)	

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

The above-referenced application is a Divisional of U.S. Serial No. 10/198,925 filed on July 22, 2002. It includes the same disclosure as U.S. patent application Serial No. 10/198,925.

It is understood that the listed references will be considered in the examination of the application and that no separate copies of the same prior art are required to be provided since they were previously cited or transmitted in the foregoing prior application, pursuant to 37 CFR § 1.98(d). Form(s) PTO 1449 is enclosed listing references cited by the Examining Attorney and submitted by applicant in the prior applications.

This Information Disclosure Statement is submitted with the above-captioned U.S. Divisional application. Accordingly, no fee is due or payable at this time.

The Examiner is requested to acknowledge consideration of the information provided in this paper in accordance with prescribed procedures.

Please charge any additional fees or credit any overpayments in connection with this paper to Deposit Account No. 08-1480.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

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Form PTO 1449 U.S. Department of commerce Patent and Trademark Office Information Disclosure Statement by Applicant	ATTY. DOCKET NUMBER HITA.0437	SERIAL NUMBER To be assigned
	APPLICANT HIGETA et al.	
	FILING DATE Concurrently herewith	GROUP 2824

U.S. Patent Documents

Examiner Initial		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	*	5,677,889	10/14/97	Haraguchi et al.			8/18/95
	*	2001/0006476 A1	7/5/2001	Itoh et al.			2/23/2001
	*	2002/0027256 A1	3/7/2002	Ishibashi et al			11/16/01
	*	6,046,627	4/4/2000	Itoh et al			2/20/98
	*	5,757,702	5/26/98	Iwata et al			10/29/96
	X	6,316,812	11/13/01	Nagaoka			05/04/00
	X	5,875,133	02/23/99	Miyashita et al			07/19/96

Foreign Patent Documents

Examiner Initial		DOCUMENT NUMBER	FILING DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
							YES	No
	*	5-120882	10/29/91	Japan			Abstract	X
	*	58-161195	3/19/82	Japan			Abstract	X
	*	2-295164	5/10/89	Japan			Abstract	X
	*	8-69693	8/30/94	Japan				X
	*	9-51042	2/15/96	Japan				X
	*	2001-15704		Japan				X
	*	WO 97/38444	4/8/97	PCT			Abstract	X
	*	10-242839	2/28/97	Japan				X
	*	3-83289	8/25/89	Japan			Abstract	X

Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)

	*	Takakuni Douseki and Shin-ichiro Mutoh, "Static-Noise Margin Analysis for a Scaled-Down CMOS Memory Cell", Journal of Institute of Electronics Information and Communication Engineers C-11, (July 1992), Vol . J75-c-11 No. 7, pp. 350-361
	*	T. Inukai, M. Takamiya, K. Nose, H. Kawaguchi, T. Hiramoto and T. Sakurai, "Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakage-Free Giga-Scale Integration", IEEE 2000 Custom Integrated Circuits Conference, pp. 409-412

EXAMINER	DATE CONSIDERED

*** Filed by Applicant in parent**
X Cited by Examiner in Parent
Examiner: Initial if citation is considered, whether or not citation is in conformance with MPEP 609; draw a line through citation if not in conformance and not considered. Include a copy of this form with next communication to applicant

PTO 1449